IN THE CLAIMS

1. (Currently Amended) An apparatus comprising:

a first transistor device including first, second, and third terminals;

a second transistor device including first, second, and third terminals;

a first impedance device to couple the second terminal of the second transistor device to the first terminal of the first transistor device; and

a second impedance device to couple the second terminal of the first transistor device to the first terminal of the second transistor device, wherein the first and second impedance devices include capacitive and resistive impedance characteristics, wherein

the first impedance device comprises a capacitive element and a resistive element, wherein each of the capacitive element and the resistive element includes first and second terminals, wherein the first terminal of the capacitive element and the first terminal of the resistive element are each coupled to the second terminal of the second transistor device, and wherein the second terminal of the capacitive element and the second terminal of the resistive element are each coupled to the first terminal of the first transistor device, and

the second impedance device comprises a capacitive element and a resistive element, wherein each of the capacitive element and the resistive element includes first and second terminals, wherein the first terminal of the capacitive element and the first terminal of the resistive element are each coupled to the second terminal of the first transistor device, and wherein the second terminal of the capacitive element and the second terminal of the resistive element are each coupled to the first terminal of the second transistor device.

2. (Original) The apparatus of Claim 1, wherein the first and second impedance devices comprise substantially the same capacitive and resistive impedance characteristics.

3. (Original) The apparatus of Claim 1, wherein a voltage build-up across the first impedance device extends a voltage peak that can be applied at the first terminal of the first transistor device and maintain an operating second terminal voltage of the second transistor device.

4. (Original) The apparatus of Claim 1, wherein a voltage build-up across the second impedance device extends a voltage peak that can be applied at the first terminal of the second transistor device and maintain an operating second terminal voltage of the first transistor device.

5. (Original) The apparatus of Claim 1, wherein the first impedance device comprises a resistive element in parallel with a capacitive element.

6. (Original) The apparatus of Claim 1, wherein the second impedance device comprises a resistive element in parallel with a capacitive element.

7. (Currently Amended) The apparatus of Claim 1, wherein a maximum output voltage swing provided between first terminals of the first and second transistor devices is based on the ~~impedance~~ impedances of the first and second impedance devices.

8. (Original) The apparatus of Claim 1, further comprising:

a first inductive element to couple the first terminal of the first transistor device to a voltage bias;

a second inductive element to couple the first terminal of the second transistor device to the voltage bias;

a capacitive element to couple the first terminal of the first transistor device to the first terminal of the second transistor device; and

a current source coupled to the third terminals of the first and second transistor devices.

Claims 9-15 (Cancelled)

16. (New) The apparatus of claim 1, wherein the first transistor device comprises a bipolar junction transistor device and wherein the second transistor device comprises a bipolar junction transistor device.

17. (New) An apparatus comprising:

a first bipolar junction transistor device including first, second, and third terminals;

a second bipolar junction transistor device including first, second, and third terminals;

a first impedance device to couple the second terminal of the second transistor device to the first terminal of the first transistor device;

a second impedance device to couple the second terminal of the first transistor device to the first terminal of the second transistor device, wherein the first and second impedance devices include capacitive and resistive impedance characteristics;

a first inductive element to couple the first terminal of the first transistor device to a voltage bias;

a second inductive element to couple the first terminal of the second transistor device to the voltage bias;

a capacitive element to couple the first terminal of the first transistor device to the first terminal of the second transistor device; and

a current source coupled to the third terminals of the first and second transistor devices, wherein

the first impedance device comprises a capacitive element and a resistive element, wherein each of the capacitive element and the resistive element includes first and second terminals, wherein the first terminal of the capacitive element and the first terminal of the resistive element are each coupled to the second terminal of the second transistor device, and wherein the second terminal of the capacitive element and the second terminal of the resistive element are each coupled to the first terminal of the first transistor device, and

the second impedance device comprises a capacitive element and a resistive element, wherein each of the capacitive element and the resistive element includes first and second terminals, wherein the first terminal of the capacitive element and the first terminal of the resistive element are each coupled to the second terminal of the first transistor device, and wherein the second terminal of the capacitive element and the second terminal of the resistive element are each coupled to the first terminal of the second transistor device.

18. (New) The apparatus of Claim 17, wherein a sinusoidal output signal is provided between the first terminal of the first bipolar junction transistor device and the first terminal of the second bipolar junction transistor device.

19. (New) The apparatus of Claim 17, wherein the first and second impedance devices comprise substantially the same capacitive and resistive impedance characteristics.

20. (New) The apparatus of Claim 17, wherein a maximum output voltage swing provided between first terminals of the first and second transistor devices is based on the impedances of the first and second impedance devices.

21. (New) A method comprising:

providing a sinusoidal signal source between a pair of terminals, wherein one of the terminals comprises a first terminal of a first transistor device and wherein another of the terminals comprises a first terminal of a second transistor device and wherein a first impedance device couples a second terminal of the second transistor device to the first terminal of the first transistor device and wherein a second impedance device couples a second terminal of the first transistor device to the first terminal of the second transistor device, and wherein:

the first impedance device comprises a capacitive element and a resistive element, wherein each of the capacitive element and the resistive element includes first and second terminals, wherein the first terminal of the capacitive element and the first terminal of the resistive element are each coupled to the second terminal of the second transistor device, and wherein the second terminal of the capacitive element and the second terminal of the resistive element are each coupled to the first terminal of the first transistor device, and

the second impedance device comprises a capacitive element and a resistive element, wherein each of the capacitive element and the resistive element includes first and second terminals, wherein the first terminal of the capacitive element and the first terminal of the resistive element are each coupled to the second terminal of the first transistor device, and wherein the second terminal of the capacitive element and the second terminal of the resistive element are each coupled to the first terminal of the second transistor device.

22. (New) The method of Claim 21, wherein the first and second impedance devices comprise substantially the same capacitive and resistive impedance characteristics.

23. (New) The method of Claim 21, wherein a maximum output voltage swing provided between first terminals of the first and second transistor devices is based on the impedances of the first and second impedance devices.

24. (New) The method of Claim 21, further comprising:

a first inductive element to couple the first terminal of the first transistor device to a voltage bias;

a second inductive element to couple the first terminal of the second transistor device to the voltage bias;

a capacitive element to couple the first terminal of the first transistor device to the first terminal of the second transistor device; and

a current source coupled to the third terminals of the first and second transistor devices.